

This listing of claims will replace all prior versions, and listings, of claims in the application:

**LISTING OF CLAIMS:**

1. (Currently Amended) A converter circuit for switching a large number of switching voltage levels, having  $n$  first switching groups  $\{1.1, \dots, 1.n\}$  which are provided for each phase (R, Y, B), with the  $n$ -th first switching group  $\{1.n\}$  being formed by a first power semiconductor switch  $\{2\}$  and a second power semiconductor switch  $\{3\}$ , and with the first first switching group  $\{1.1\}$  to the  $(n-1)$ -th switching group  $\{1.(n-1)\}$  each being formed by a first power semiconductor switch  $\{2\}$  and a second power semiconductor switch  $\{3\}$  and by a capacitor  $\{4\}$ , which is connected to the first and second power semiconductor switches  $\{2, 3\}$ , with each of the  $n$  first switching groups  $\{1.1, \dots, 1.n\}$  being connected in series to the respectively adjacent first switching group  $\{1.1, \dots, 1.n\}$ , and with the first and the second power semiconductor switches  $\{2, 3\}$  in the first first switching group  $\{1.1\}$  being connected to one another, ~~characterized in that~~ wherein  $n \geq 1$  and  $p$  second switching groups  $\{5.1, \dots, 5.p\}$  and  $p$  third switching groups  $\{6.1, \dots, 6.p\}$  are provided, which are each formed by a first power semiconductor switch  $\{2\}$  and a second power semiconductor switch  $\{3\}$  and by a capacitor  $\{4\}$  which is connected to the first and second power semiconductor switches  $\{2, 3\}$ , where  $p \geq 1$  and each of the  $p$  second switching groups  $\{5.1, \dots, 5.p\}$  is connected in series with the respectively adjacent second switching group  $\{5.1, \dots, 5.p\}$ , and each of the  $p$  third switching groups  $\{6.1, \dots, 6.p\}$  is connected in series with the respectively adjacent third switching group  $\{6.1, \dots, 6.p\}$ , and the first second switching group  $\{5.1\}$  is connected to the first power semiconductor switch  $\{2\}$  in the  $n$ -th first switching group  $\{1.n\}$ , and the first third switching group  $\{6.1\}$  is connected to the second power semiconductor switch  $\{3\}$  in the  $n$ -th first switching group  $\{1.n\}$ , and in that the capacitor  $\{4\}$  in the  $p$ -th second switching group  $\{5.p\}$  is connected in series with the capacitor  $\{4\}$  in the  $p$ -th third switching group  $\{6.p\}$ .

2. (Currently Amended) The converter circuit as claimed in claim 1, ~~characterized in that~~ wherein a voltage limiting network (7) is connected in parallel with the first power semiconductor switch (2) in the n-th first switching group (1-n), and in that a voltage limiting network (7) is connected in parallel with the second power semiconductor switch (3) in the n-th first switching group (1-n).

3. (Currently Amended) The converter circuit as claimed in claim 2, ~~characterized in that~~ wherein the voltage limiting network (7) has a capacitor.

4. (Currently Amended) The converter circuit as claimed in claim 2, ~~characterized in that~~ wherein the voltage limiting network (7) has a series circuit formed by a resistor with a capacitor.

5. (Currently Amended) The converter circuit as claimed in claim 1, ~~characterized in that~~ wherein the n-th first switching group (1-n) has a capacitor (4) which is connected to the first and second power semiconductor switches (2, 3) in the n-th first switching group (1-n), with the first second switching group (5-1) being connected to the capacitor (4) in the n-th first switching group (1-n), and with the first third switching group (6-1) being connected to the capacitor (4) in the n-th first switching group (1-n).

6. (Currently Amended) The converter circuit as claimed in ~~one of claims 1 to 4~~ claim 1, ~~characterized in that~~ wherein the first and second power semiconductor switches (2, 3) in the first second switching group (5-1) are connected to one another, with the junction point of the first and second power semiconductor switches (2, 3) in the first second switching group (5-1) being connected to the first power semiconductor switch (2) in the n-th first switching group (1-n), and in that the first and second power semiconductor switches (2, 3) in the first third switching group (6-1) are connected to one another, with the junction point of the first and second power semiconductor switches (2, 3) in the first third switching group (6-1) being connected to the second power semiconductor switch (3) in the n-th first switching group (1-n).

7. (Currently Amended) The converter circuit as claimed in claim 5, ~~characterized in that~~ wherein the first and second power semiconductor switches (2, 3) in the first second switching group (5.1) are connected to one another, with the junction point of the first and second power semiconductor switches (2, 3) in the first second switching group (5.1) being connected to the junction point of the capacitor (4) in the n-th first switching group (1.n) and the first power semiconductor switch (2) in the n-th first switching group (1.n), and in that the first and second power semiconductor switches (2, 3) in the first third switching group (6.1) are connected to one another, with the junction point of the first and second power semiconductor switches (2, 3) in the first third switching group (6.1) being connected to the junction point of the capacitor (4) in the n-th first switching group (1.n) and the second power semiconductor switch (3) in the n-th first switching group (1.n).

8. (Currently Amended) The converter circuit as claimed in ~~one of claims 1 to 7~~ claim 1, ~~characterized in that~~ wherein the total number of then first switching groups (1.1, ..., 1.n) corresponds to the total number of the p second and third switching groups (5.1, ..., 5.p; 6.1, ..., 6.p).

9. (Currently Amended) The converter circuit as claimed in ~~one of claims 1 to 7~~ claim 1, ~~characterized in that~~ wherein the total number of the n first switching groups (1.1, ..., 1.n) is less than the total number of the p second and third switching groups (5.1, ..., 5.p; 6.1, ..., 6.p).

10. (Currently Amended) The converter circuit as claimed in ~~one of claims 1 to 7~~ claim 1, ~~characterized in that~~ wherein the total number of the n first switching groups (1.1, ..., 1.n) is greater than the total number of the p second and third switching groups (5.1, ..., 5.p; 6.1, ..., 6.p).

11. (Currently Amended) The converter circuit as claimed in ~~one of claims 1 to 10~~ claim 1, ~~characterized in that~~ wherein the first power semiconductor switch (2) and the second power semiconductor switch (3) in each switching group (1.1, ..., 1.n;

5.1, ..., 5.p; 6.1, ..., 6.p) are in each case in the form of a bidirectional power semiconductor switch.

12. (Currently Amended) The converter circuit as claimed in ~~one of claims 1 to 10~~ claim 1, ~~characterized in that~~ wherein the first power semiconductor switch (2) in each first and in each second switching group (1.1, ..., 1.n; 5.1, ..., 5.p) is a bidirectional power semiconductor switch, ~~in that~~ wherein the second power semiconductor switch (3) in each first and in each third switching group (1.1, ..., 1.n; 6.1, ..., 6.p) is a bidirectional power semiconductor switch, and ~~in that~~ wherein the second power semiconductor switch (3) in each second switching group (5.1, ..., 5.p) and the first power semiconductor switch (2) in each third switching group (6.1, ..., 6.p) are in each case in the form of a unidirectional power semiconductor switch.

13. (Currently Amended) The converter circuit as claimed in ~~one of claims 1 to 10~~ claim 1, ~~characterized in that~~ wherein the first power semiconductor switch (2) in each first and in each third switching group (1.1, ..., 1.n; 6.1, ..., 6.p) is a bidirectional power semiconductor switch, ~~in that~~ wherein the second power semiconductor switch (3) in each first and in each second switching group (1.1, ..., 1.n; 5.1, ..., 5.p) is a bidirectional power semiconductor switch, and ~~in that~~ wherein the first power semiconductor switch (2) in each second switching group (5.1, ..., 5.p) and the second power semiconductor switch (3) in each third switching group (6.1, ..., 6.p) is a unidirectional power semiconductor switch.

14. (Currently Amended) The converter circuit as claimed in ~~one of claims 1 to 10~~ claim 1, ~~characterized in that~~ wherein the first power semiconductor switch (2) and the second power semiconductor switch (3) in each first switching group (1.1, ..., 1.n) are in each case in the form of a bidirectional power semiconductor switch, and ~~in that~~ wherein the first power semiconductor switch (2) and the second power semiconductor switch (3) in each second switching group (5.1, ..., 5.p) and in each third switching group (6.1, ..., 6.p) are in each case in the form of a unidirectional power semiconductor switch.

15. (Currently Amended) The converter circuit as claimed in ~~one of claims 11 to 14~~ claim 11, ~~characterized in that~~ wherein the bidirectional power semiconductor switch is formed by an electronic component which can be driven and carries current in only one direction, and by a passive electronic component which is connected back-to-back in parallel with this, cannot be driven and carries current in only one direction.

16. (Currently Amended) The converter circuit as claimed in ~~one of claims 12 to 15~~ claim 12, ~~characterized in that~~ wherein the unidirectional power semiconductor switch is formed by a passive electronic component which cannot be driven and carries current in only one direction.

17. (Currently Amended) The converter circuit as claimed in ~~one of the preceding claims~~ claim 1, ~~characterized in that~~ wherein, in the case of the  $n$  first switching groups  $\{1.1, \dots, 1.n\}$ , the two first power semiconductor switches  $\{2\}$  in respectively adjacent first switching groups  $\{1.1, \dots, 1.n\}$  are integrated in a module, and the two second power semiconductor switches  $\{3\}$  in respectively adjacent first switching groups  $\{1.1, \dots, 1.n\}$  are integrated in a module.

18. (Currently Amended) The converter circuit as claimed in claim 17, ~~characterized in that~~ wherein, in the case of the  $p$  second switching groups  $\{5.1, \dots, 5.p\}$ , the two first power semiconductor switches  $\{2\}$  in respectively adjacent second switching groups  $\{5.1, \dots, 5.p\}$  are integrated in a module, and the two second power semiconductor switches  $\{3\}$  in respectively adjacent second switching groups  $\{5.1, \dots, 5.p\}$  are integrated in a module, and ~~in that~~ wherein, in the case of the  $p$  third switching groups  $\{6.1, \dots, 6.p\}$ , the two first power semiconductor switches  $\{2\}$  in respectively adjacent third switching groups  $\{6.1, \dots, 6.p\}$  are integrated in a module, and the two second power semiconductor switches  $\{3\}$  in respectively adjacent third switching groups  $\{6.1, \dots, 6.p\}$  are integrated in a module.

19. (Currently Amended) The converter circuit as claimed in ~~one of~~ ~~claims 1 to 16~~ claim 1, ~~characterized in that~~ wherein, in the case of the n first switching groups  $\{1.1, \dots, 1.n\}$  and in the case of the p second and third switching groups  $\{5.1, \dots, 5.p; 6.1, \dots, 6.p\}$ , the first power semiconductor switch (2) and the second power semiconductor switch (3) are in each case integrated in a module.

20. (Currently Amended) The converter circuit as claimed in ~~one of~~ ~~the preceding claims~~ claim 1, ~~characterized in that~~ wherein, if there are a plurality of phases (R, Y, B), the p-th second switching groups  $\{5.p\}$  for the phases (R, Y, B) are connected in parallel with one another, and the p-th third switching groups  $\{6.p\}$  for the phases (R, Y, B) are connected in parallel with one another.

21. (Currently Amended) The converter circuit as claimed in claim 20, ~~characterized in that~~ wherein the capacitors (4) in the p-th second switching groups  $\{5.p\}$  for the phases (R, Y, B) are combined to form one capacitor, and ~~in that~~ wherein the capacitors (4) in the p-th third switching groups  $\{6.p\}$  for the phases (R, Y, B) are combined to form one capacitor.